

cells are formed, and having connector terminals to be connected to upper wiring layers; and

upper wirings in predetermined wiring directions and in predetermined wiring widths both appropriately selected, for connecting, in the upper wiring layers, the corresponding connector terminals of the fundamental cell.

*B2*  

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21. (New) A semiconductor integrated circuit, comprising:

a first hierarchy where a plurality of fundamental cells and a plurality of connector terminals are formed, wherein metal wirings other than power supply wirings are formed; and

*B3*  
a second hierarchy, provided above the first hierarchy, where fixed power supplies are formed;

*LK1*  
wherein the plurality of fundamental cells and the fixed power supplies are connected via the plurality of connector terminals.

*LK2*  
22. (New) A fundamental cell, used as a basic unit in layout of a semiconductor integrated circuit, comprising:

no fixed wiring for commonly wiring between fundamental cells in a plane pattern where fundamental cells are formed, and  
connector terminals to be connected to upper wiring layers.

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A marked-up version of the amended claims is enclosed as required by 37 C.F.R. § 1.121.